

REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

FIGs. 1 and 9 stand objected to.. In response, claims 17, 21-25, and 63-64 are amended to remove this objected-to language.

The drawings stand objected to based on not showing the thinning region of the TFT substrate of FIGs. 12 and 43. These claims are canceled herewith.

The specification stands objected to as allegedly failing to provide a proper antecedent basis for the claimed subject matter of claims 2, 45-50, and 17. Claims 45-50 are canceled to obviate this rejection.

Claims 2, 10, 27, 32, and 37 stand rejected under 35 U.S.C. 112, second paragraph. These claims are amended herewith for definiteness. The also objected-to claims 5, 29, 34, and 39 are canceled to obviate the rejections thereto.

Claims 24 and 25 stand rejected under 35 U.S.C. 12, second paragraph. These claims are amended herewith to obviate the rejection.

Claims 61-64 and 69-72 stand rejected under 35 U.S.C. 103(a) as allegedly being obvious over the admitted prior art in view of Inoue, McClelland, and Sasaki. These claims are amended

to recite that the gate insulating film has a thickness of between 500 Å and 2000 Å. This should obviate the rejection.

Claims 2, 4-6, 10, 12-14, 17, and 21-56 stand rejected over the admitted prior art in view of Inoue, McClelland, Sasaki, and further in view of the Japanese document 555 or the Japanese document 446. In response, claims 17, 21, 22, 23, 24, and 25 are amended to recite that the control circuit is provided over the first substrate and in this way that the pixel TFTs and the driver TFTs and the control circuit are provided over the first substrate.

Claims 2, 4-6, 10, 12-14, 17, and 21-56 stand rejected based on judicially created obviousness-type double patenting. Claims 17 and 21-25 are amended in response to the rejection and it is respectfully suggested that the double patenting rejection is no longer applicable to these amended claims. The remaining claims are all either dependent claims or canceled, and thus, it is respectfully suggested that this obviates the rejection.

In view of the above amendments and remarks, therefore, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

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Respectfully submitted,

Date: _____

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VERSION TO SHOW CHANGES MADE

In the Claims:

Claims 5, 12, 26, 28, 29, 33, 34, 38, 39, 43, and 45-50 have been canceled.

The claims have been amended as follows.

2. (Amended) The display of claim 17, wherein a direction of array of said pixel TFTs is parallel or vertical to said side edge of said [TFT] first substrate to which said nonconductive or weakly conductive material is applied or adhesively bonded [is parallel or vertical to a direction of array of said pixel TFTs].

6. (Amended) The display of claim 17, wherein said control circuit is packed over said [TFT] first substrate by COG (chip-on-glass) technology.

10. (Amended) The method of claim 24, wherein said cutting step is carried out in such a way that a direction of array of said pixel TFTs is parallel or vertical to said cut [end surfaces] side edges to which said nonconductive or weakly conductive material is applied or adhesively bonded [are

parallel or vertical to a direction of array of said pixel TFTs].

14. (Amended) The method of claim 24, wherein said control circuit is packed over said [TFT] first substrate by COG (chip-on-glass) technology.

17. (Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a [TFT] first substrate and arrayed in a matrix;

driver TFTs ^{a driver circuit} formed over said [TFT] first substrate [and forming a driver circuit] for driving said pixel TFTs;

a bus line provided over said [TFT] first substrate and connected with at least one of said pixel TFTs;

[a layer of a liquid crystal material with which said pixel TFTs and driver TFTs are in contact directly or via a thin film;]

a counter substrate located opposite to said [TFT] first substrate;

a nonconductive or weakly conductive material applied or adhesively bonded to a side edge of said counter substrate and a side edge of said [TFT] first substrate;

a sealing material provided between said [TFT] first substrate and said counter substrate and inside said side edge of said counter substrate and said side edge of said [TFT] first substrate; and

a control circuit comprising a semiconductor chip provided under and in contact with said sealing material for controlling said driver circuit, ⁹⁰¹ said control circuit provided over said first substrate. *Fig 9*

21. (Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a [TFT] first substrate and arrayed in a matrix;

driver TFTs formed over said [TFT] first substrate and forming a driver circuit for driving said pixel TFTs;

a bus line provided over said [TFT] first substrate and connected with at least one of said pixel TFTs;

[a layer of a liquid crystal material with which said pixel TFTs and driver TFTs are in contact directly or via a thin film;]

a counter substrate located opposite to said [TFT] first substrate;

a nonconductive or weakly conductive material applied or adhesively bonded to a side edge of said counter substrate and a side edge of said [TFT] first substrate;

a sealing material provided between said [TFT] first substrate and said counter substrate and inside said side edge of said counter substrate and said side edge of said [TFT] first substrate; and

a control circuit comprising a semiconductor chip provided under and in contact with said sealing material for controlling said driver circuit, said control circuit provided over said first substrate.

22.(Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a [TFT] first substrate and arrayed in a matrix;

driver TFTs formed over said [TFT] first substrate and forming a driver circuit for driving said pixel TFTs;

a bus line provided over said [TFT] first substrate and connected with at least one of said pixel TFTs;

[a layer of a liquid crystal material with which said pixel TFTs and driver TFTs are in contact directly or via a thin film;]

a counter substrate located opposite to said [TFT] first substrate;

a nonconductive or weakly conductive material applied or adhesively bonded to a side edge of said counter substrate and a side edge of said [TFT] first substrate;

a sealing material provided between said [TFT] first substrate and said counter substrate and inside said side edge of said counter substrate and said side edge of said [TFT] first substrate, said sealing material being provided outside at least said pixel TFTs; and

a control circuit comprising a semiconductor chip provided under and in contact with said sealing material for controlling said driver circuit, said control circuit provided over said first substrate.

23. (Amended) An active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a [TFT] first substrate and arrayed in a matrix;

driver TFTs formed over said [TFT] first substrate and forming a driver circuit for driving said pixel TFTs;

a bus line provided over said [TFT] first substrate and connected with at least one of said pixel TFTs;

[a layer of a liquid crystal material with which said pixel TFTs and driver TFTs are in contact directly or via a thin film;]

a counter substrate located opposite to said [TFT] first substrate;

a nonconductive or weakly conductive material applied or adhesively bonded to a side edge of said counter substrate and a side edge of said [TFT] first substrate;

a sealing material provided between said [TFT] first substrate and said counter substrate and inside said side edge of said counter substrate and said side edge of said [TFT] first substrate, said sealing material being provided outside said pixel TFTs and said driver TFTs; and

a control circuit comprising a semiconductor chip provided under and in contact with said sealing material for controlling said driver circuit, said control circuit provided over said first substrate.

24. (Amended) A method of fabricating an active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a [TFT] first substrate and arrayed in a matrix;

driver TFTs formed over said [TFT] first substrate and forming a driver circuit for driving said pixel TFTs;

a bus line provided over said [TFT] first substrate and connected with at least one of said pixel TFTs;

[a layer of a liquid crystal material with which said pixel TFTs and driver TFTs are in contact directly or via a thin film;]

a counter substrate located opposite to said [TFT] first substrate;

a sealing material provided between said [TFT] first substrate and said counter substrate and outside at least said pixel TFTs; and

a control circuit comprising a semiconductor chip provided under and in contact with said sealing material for controlling said driver circuit, said control circuit provided over said first substrate,

said method comprising:

cutting said [TFT] first substrate and said counter substrate at a cut side edge of said first substrate and at a cut side edge of said counter substrate outside said sealing material having said control circuit under and in contact with said sealing material; and

applying or adhesively bonding a nonconductive or weakly conductive material to the cut side edge of said [TFT] first substrate and the cut side edge of said counter substrate.

25. (Amended) A method of fabricating an active matrix liquid crystal display comprising:

a plurality of pixel TFTs arranged in rows and columns over a [TFT] first substrate and arrayed in a matrix;

driver TFTs formed over said [TFT] first substrate and forming a driver circuit for driving said pixel TFTs;

a bus line provided over said [TFT] first substrate and connected with at least one of said pixel TFTs;

[a layer of a liquid crystal material with which said pixel TFTs and driver TFTs are in contact directly or via a thin film;]

a counter substrate located opposite to said [TFT] first substrate;

a sealing material provided between said [TFT] first substrate and said counter substrate and outside said pixel TFTs and said driver TFTs; and

a control circuit comprising a semiconductor chip provided under and in contact with said sealing material for controlling said driver circuit, said control circuit provided over said first substrate,

said method comprising:

cutting said [TFT] first substrate and said counter substrate at a cut side edge of said first substrate and at a cut side edge of said counter substrate outside said sealing

material having said control circuit under and in contact with said sealing material; and

applying or adhesively bonding a nonconductive or weakly conductive material to the cut side edge of said [TFT] first substrate and the cut side edge of said counter substrate.

27. (Amended) The display of claim 21, wherein a direction of array of said pixel TFTs is parallel or vertical to said side edge of said [TFT] first substrate to which said nonconductive or weakly conductive material is applied or adhesively bonded [is parallel or vertical to a direction of array of said pixel TFTs].

31. (Amended) The display of claim 21, wherein said control circuit is packed over said [TFT] first substrate by COG (chip-on-glass) technology.

32. (Amended) The display of claim 22, wherein a direction of array of said pixel TFTs is parallel or vertical to said side edge of said [TFT] first substrate to which said nonconductive or weakly conductive material is applied or adhesively bonded [is parallel or vertical to a direction of array of said pixel TFTs].

36.(Amended) The display of claim 22, wherein said control circuit is packed over said [TFT] first substrate by COG (chip-on-glass) technology.

37.(Amended) The display of claim 23, wherein a direction of array of said pixel TFTs is parallel or vertical to said side edge of said [TFT] first substrate to which said nonconductive or weakly conductive material is applied or adhesively bonded [is parallel or vertical to a direction of array of said pixel TFTs].

41.(Amended) The display of claim 23, wherein said control circuit is packed over said [TFT] first substrate by COG (chip-on-glass) technology.

51.(Amended) The display of claim 17, wherein said sealing material is apart from said side edge of said counter substrate and said side edge of said [TFT] first substrate.

52.(Amended) The display of claim 21, wherein said sealing material is apart from said side edge of said counter substrate and said side edge of said [TFT] first substrate.

53. (Amended) The display of claim 22, wherein said sealing material is apart from said side edge of said counter substrate and said side edge of said [TFT] first substrate.

54. (Amended) The display of claim 23, wherein said sealing material is apart from said side edge of said counter substrate and said side edge of said [TFT] first substrate.

55. (Amended) The method of claim 24, wherein said sealing material is apart from ¹¹²⁹said side edge of said counter substrate and said side edge of said [TFT] first substrate.

56. (Amended) The method of claim 25, wherein said sealing material is apart from said side edge of said counter substrate and said side edge of said [TFT] first substrate.

61. (Amended) A semiconductor device comprising:

a pixel TFT provided over a [TFT] first substrate
comprising a glass;

a channel formation region provided in a semiconductor film
provided over said first substrate;

a gate electrode provided adjacent to said channel
formation region with a gate insulating film therebetween;

a counter substrate located opposite to said [TFT] first
substrate;

a bus line provided over said [TFT] first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said [TFT] first substrate;

a sealing material provided between said [TFT] first substrate and said counter substrate; and

a nonconductive material applied to a side edge of said counter substrate and said side edge of said [TFT] first substrate and said part of said bus line,

wherein said nonconductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

62. (Amended) A semiconductor device comprising:

a pixel TFT provided over a [TFT] first substrate comprising a glass;

a channel formation region provided in a semiconductor film provided over said first substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween;

a counter substrate located opposite to said [TFT] first substrate;

a bus line provided over said [TFT] first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said [TFT] first substrate;

a sealing material provided between said [TFT] first substrate and said counter substrate; and

a weakly conductive material applied to a side edge of said counter substrate and said side edge of said [TFT] first substrate and said part of said bus line,

wherein said weakly conductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

63. (Amended) A semiconductor device comprising:

a pixel TFT provided over a [TFT] first substrate comprising a glass;

a channel formation region provided in a semiconductor film provided over said first substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween;

a driver TFT provided over said [TFT] first substrate;

[a layer of a liquid crystal material with which said pixel TFT and said driver TFT are in contact directly or via a thin film;]

a counter substrate located opposite to said [TFT] first substrate [with said layer of the liquid crystal material therebetween];

a bus line provided over said [TFT] first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said [TFT] first substrate;

a sealing material provided between said [TFT] first substrate and said counter substrate; and

a nonconductive material applied to a side edge of said counter substrate and said side edge of said [TFT] first substrate and said part of said bus line,

wherein said nonconductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

64. (Amended) A semiconductor device comprising:

a pixel TFT provided over a [TFT] first substrate comprising a glass;

a channel formation region provided in a semiconductor film provided over said first substrate;

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween;

a driver TFT provided over said [TFT] first substrate;

[a layer of a liquid crystal material with which said pixel TFT and said driver TFT are in contact directly or via a thin film;]

a counter substrate located opposite to said [TFT] first substrate [with said layer of the liquid crystal material therebetween];

a bus line provided over said [TFT] first substrate and connected with said pixel TFT, said bus line having a part located adjacent to a side edge of said [TFT] first substrate;

a sealing material provided between said [TFT] first substrate and said counter substrate; and

a weakly conductive material applied to a side edge of said counter substrate and said side edge of said [TFT] first substrate and said part of said bus line,

wherein said weakly conductive material is provided on an outer side of said sealing material, and

wherein said gate insulating film has a thickness of 500 to 2000 Å.

65. (Amended) The display of claim 17 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said [TFT] first substrate.

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66. (Amended) The display of claim 21 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said [TFT] first substrate.

67. (Amended) The display of claim 22 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said [TFT] first substrate.

68. (Amended) The display of claim 23 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said [TFT] first substrate.

69. (Amended) The display of claim 61 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said [TFT] first substrate.

70. (Amended) The display of claim 62 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said [TFT] first substrate.

71. (Amended) The display of claim 63 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said [TFT] first substrate.

72.(Amended) The display of claim 64 wherein said part of said bus line is aligned with said side edge of said counter substrate and said side edge of said [TFT] first substrate.